A 0.3 TO 3 GHz MONOLITHIC VECTOR MODULATOR FOR ADAPTIVE ARRAY SYSTEMS

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ABSTRACT

A monolithic vector modulator element has been demonstrated that combines the bi-phase modulation and gain control functions on a single chip covering the 0.3 to 3 GHz frequency band. Over 50 dB of gain control is provided.

INTRODUCTION

Adaptive Array Systems provide the unique system capability of optimizing their patterns in real time for operation in a rapidly changing RF environment. This capability will make the Adaptive Array an integral part in many future Radar and EW Systems.

Pattern optimization of the Adaptive Array is typically achieved through dithering, which involves slightly varying the amplitude and phase of the individual elements to improve performance. Dither is typically accomplished by varying the amplitude of the I and/or Q channel of the Vector Modulator via the control voltage. Dither typically requires high-speed D/A Converters to control the I and Q channels of the Vector Modulator. To reduce the speed requirement of the DAC, this MMIC (shown in Figure 1) was designed to serve as not only an I or Q channel element, but as a Dither Generator as well. An RF signal is generated in and out of phase with the I and Q channel RF. This signal is then combined with the output of the I or Q channel to create the Dither. Dither frequencies above 15 MHz have been achieved with this technique.

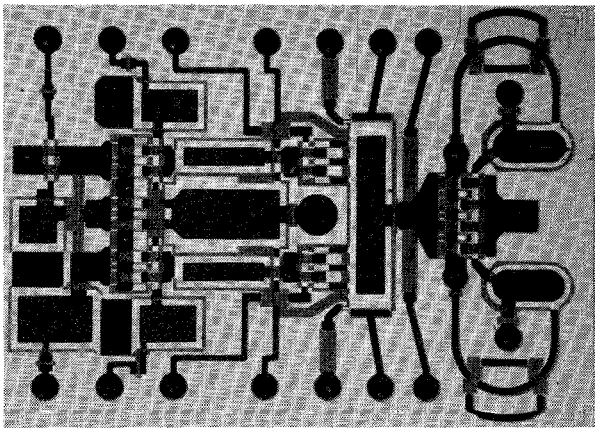

Figure 1. Monolithic Vector Modulator MMIC.

IMPLEMENTATION

The Bi-phase Modulator consists of a differential amplifier with one of the RF inputs grounded through an on-chip capacitor. The differential outputs are loaded into 25 ohm resistors which also bring in the bias. Larger resistors would have resulted in higher gain, but the bandwidth of the MMIC would have been reduced and the differential amplifier would not be saturated with a 5-volt supply. Application of the MMIC would be limited with the larger resistors, since the Common Mode Rejection Ration (CMRR), and not the gain, is considered the important feature of the MMIC. The DGFETs provide a higher output impedance and allow the differential amplifier to be adjusted to achieve CMRRs of 25 dB or better with a resistor, by varying the gate 2 bias of the 0 and 180 degree outputs. The outputs of the differential amplifier are selected by an SPDT FET switch. The switches are DC isolated with blocking capacitors on the input and output and biased to 5-volts via a bleeder resistor allowing the use of CMOS and TTL controllers. Dither is achieved by complementary pulsing of the 0 and 180 degree select switches. The switches are summed into a 600 micron Dual Gate FET (DGFET) which has its source inductively tuned to minimize the phase shift as the gain is varied.

Gain variation is achieved by varying the voltage on the second gate of the DGFET and the gate of the current source of the differential amplifier. This approach allows a greater dynamic range with less phase shift than would changing the gain with the DGFET. A more linear control voltage versus gain curve is achieved as well. The DGFET has a negative phase shift as its gain is reduced. This phase shift is compensated for by adding inductance to the source. The differential amplifier experiences a positive phase shift as it is attenuated, thus helping to cancel the negative phase shift of the DGFET.

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MMIC DESCRIPTION

The differential amplifier consists of two 400 micron RF signal DGFETs and a 400 micron current source. The gate-2's of the signal DGFETs are tied together with a 5000 ohm resistor, and terminated by a 10 pF capacitor. All gates are 2 micron for producibility considerations. One of the inputs to the differential amplifier is RF grounded using a 15 pF capacitor. The gate of the current source is terminated with a 7 pF capacitor. The differential amplifier outputs are loaded with 25 ohm resistors and a 25 pF capacitor. This loading serves to isolate the differential amplifiers outputs which are switched with 400 micron FETs. The switches are biased to 5 volts through an 8000 ohm bleeder resistor for TTL or CMOS logic control. Two 7 pF capacitors DC isolate the switches from the outputs of the differential amplifier. The switches are summed into a 27 pF capacitor. The gates of the switch FETs have a series 200 ohm resistor to decouple them from the control lines. The switches are summed into a 600 micron DGFET with an adjustable source inductor to provide phase compensation over the gain control range of the DGFET. The inductance is nominally 0 3 nH which achieves the minimum phase shift over the control range of the MMIC. A plating mask change allows the source inductor to be changed for a production run of the MMIC Drain bias for the DGFET is brought in through the RF output. The second gate of the DGFET is terminated with 15 pF of capacitance with a 200 ohm resistor in series with the control line to decouple the circuit. The chip size is roughly 80 mils by 110 mils on 6 mil GaAs.

RF PERFORMANCE

The inputs and outputs of the MMIC are unmatched to allow the greatest flexibility in circuit implementation. The measured S-parameters indicate maximum stable gain greater than 0 dB up to 5 GHz. The Common Mode Rejection to 6 GHz of the MMIC is 25 dB or better and can be achieved with the DGFET adjustment. The gain control of the DGFET exceeds 30 dB and the differential amplifier exceeds 15 dB over the 5 GHz band. Phase resolution of 0.5 degrees is possible with 42 dB of gain control. Figure 2 shows the gain of the 0° and 180° outputs of the MMIC into 50 ohms. Figure 3 shows the phase difference between the 0° and 180° outputs for an unadjusted MMIC.

CONCLUSIONS

A Vector Modulator MMIC has been developed that can be used in Adaptive Array Systems operating in the frequency range of .3 to 3 GHz with excellent RF characteristics. The MMIC is designed to provide the Vector Modulation function in numerous current and future phase array systems.

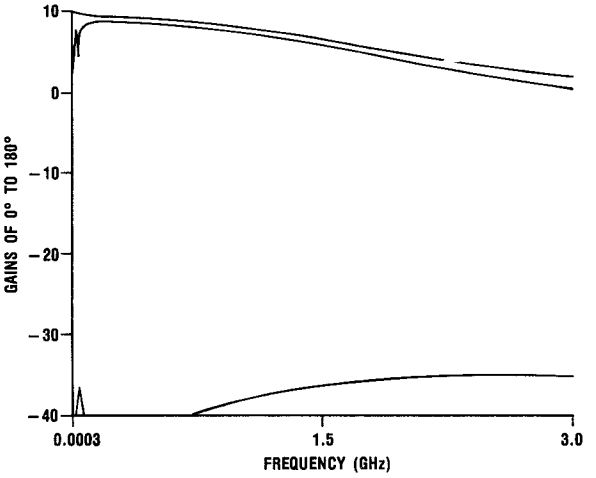

Figure 2. Gain of the 0° and 180° Outputs.

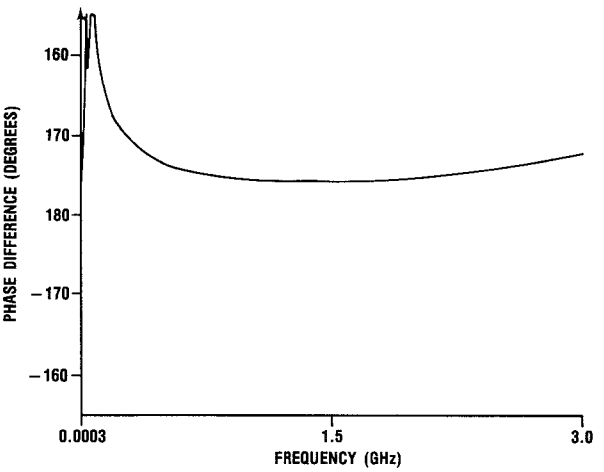

Figure 3. Phase Difference Between the 0° and 180° Outputs.

ACKNOWLEDGEMENT

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